查询X28C010供应商

# 1M X28C010 128K x 8 Bit

## 5 Volt, Byte Alterable E²PROM

### FEATURES

- Access Time: 120ns
- Simple Byte and Page Write
  - —Single 5V Supply
  - —No External High Voltages or $V_{PP}$ Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS:
  - —Active: 50mA
  - —Standby: 500µA
- Software Data Protection
  - —Protects Data Against System Level Inadvertant Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - —Endurance: 100,000 Write Cycles
  - —Data Retention: 100 Years
- Early End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit Polling

### DESCRIPTION

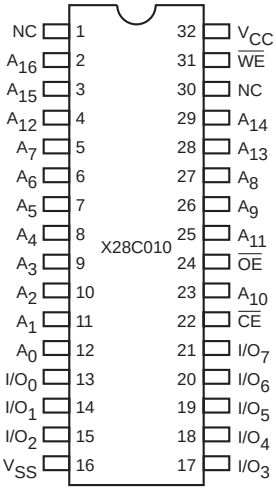
The Xicor X28C010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C010 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports Software Data Protection option.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

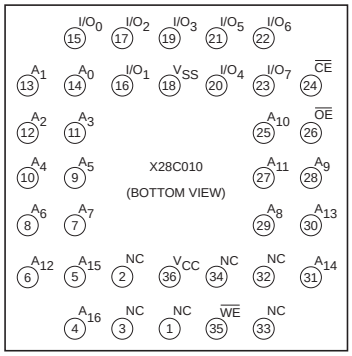
### PIN CONFIGURATIONS

CERDIP
FLAT PACK
SOIC (R)



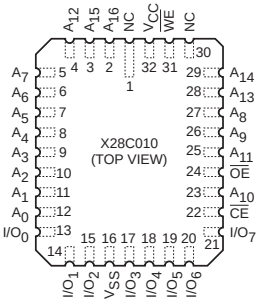

3858 FHD F02.1

PGA

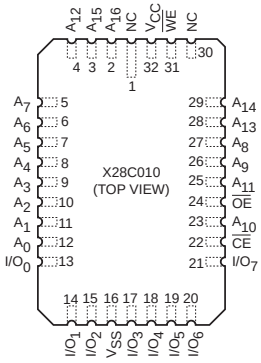

I/O0 I/O2 I/O3 I/O5 I/O6
A1 A0 I/O1 VSS I/O4 I/O7 CE
A2 A3 A10 OE
A4 A5 A11 A9
A6 A7 A8 A13
A12 A15 NC VCC NC NC A14
A16 NC NC WE NC
X28C010
(BOTTOM VIEW)

3858 FHD F20

PLCC
LCC

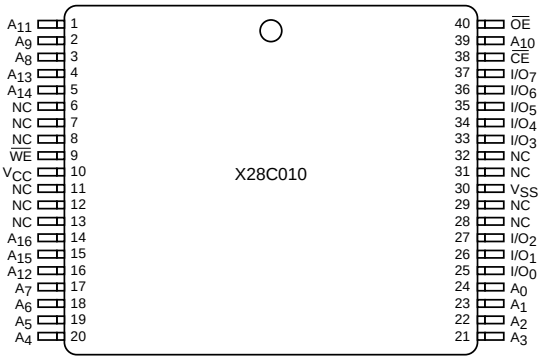



EXTENDED LCC




3858 FHD F03.1

TSOP


A11 A9 A8 A13 A14 NC NC NC WE VCC NC NC NC A16 A15 A12 A7 A6 A5 A4
OE A10 CE I/O7 I/O6 I/O5 I/O4 I/O3 NC NC VSS NC NC I/O2 I/O1 I/O0 A0 A1 A2 A3
X28C010

3858 ILL F21

© Xicor, Inc. 1991, 1995, 1996 Patents Pending

## PIN DESCRIPTIONS

### Addresses ($A_0$–$A_{16}$)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

### Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out ($I/O_0$–$I/O_7$)

Data is written to or read from the X28C010 through the I/O pins.

### Write Enable ($\overline{WE}$)

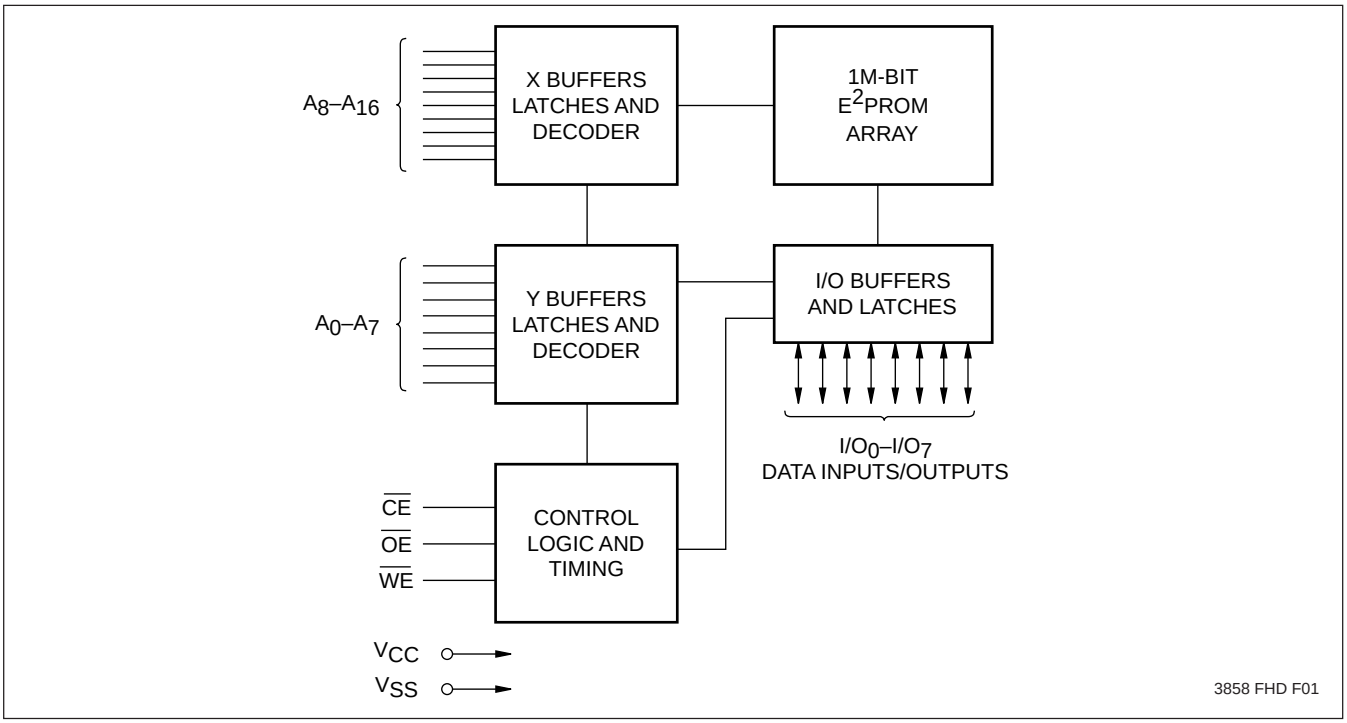
The Write Enable input controls the writing of data to the X28C010.

## PIN NAMES

| Symbol | Description |
|---|---|
| $A_0$–$A_{16}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

3858 PGM T01

## FUNCTIONAL DIAGRAM



## DEVICE OPERATION

### Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

### Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

### Page Write Operation

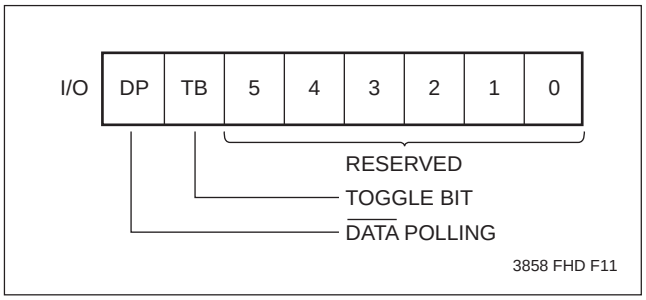
The page write feature of the X28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address ($A_8$ through $A_{16}$) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

### Write Operation Status Bits

The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

**Figure 1. Status Bit Assignment**




### $\overline{DATA}$ Polling ($I/O_7$)

The X28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on $I/O_7$ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, $I/O_7$ will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

### Toggle Bit ($I/O_6$)

The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, $I/O_6$ will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

## $\overline{DATA}$ Polling I/O$_7$

**Figure 2. $\overline{DATA}$ Polling Bus Sequence**

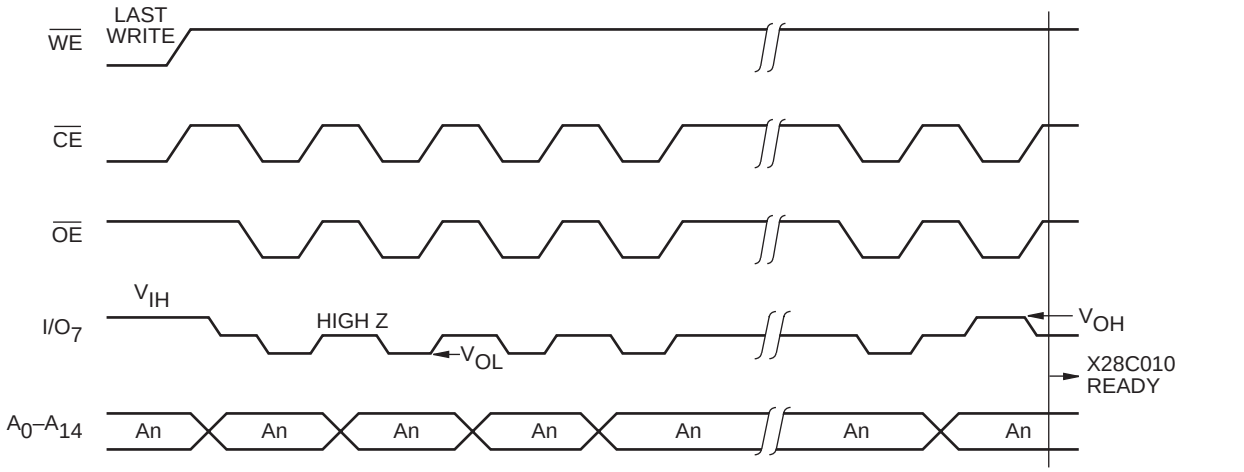
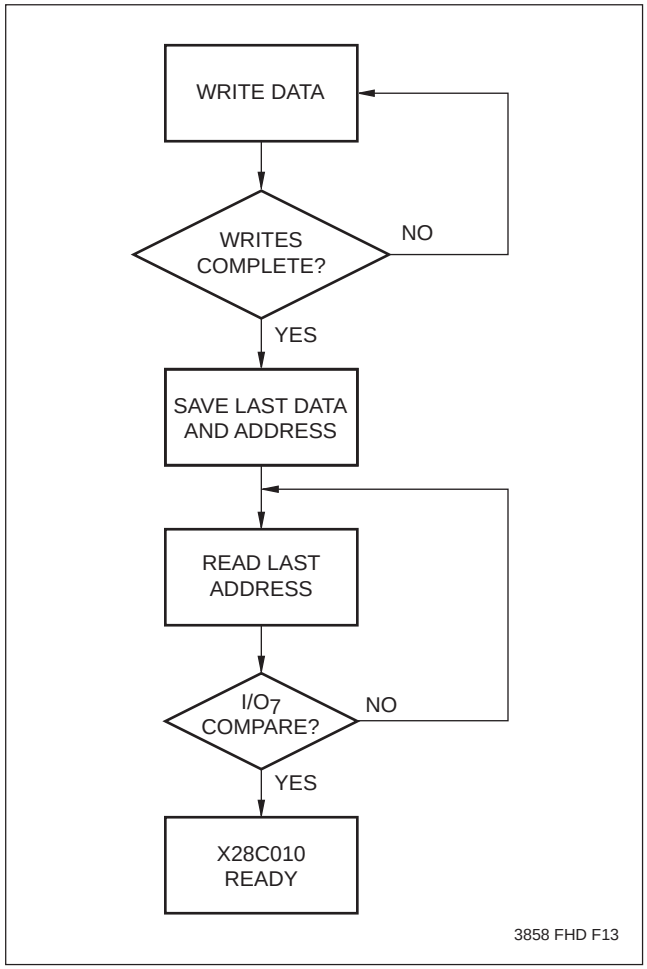



**Figure 3. $\overline{DATA}$ Polling Software Flow**




$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

### The Toggle Bit $I/O_6$

**Figure 4. Toggle Bit Bus Sequence**

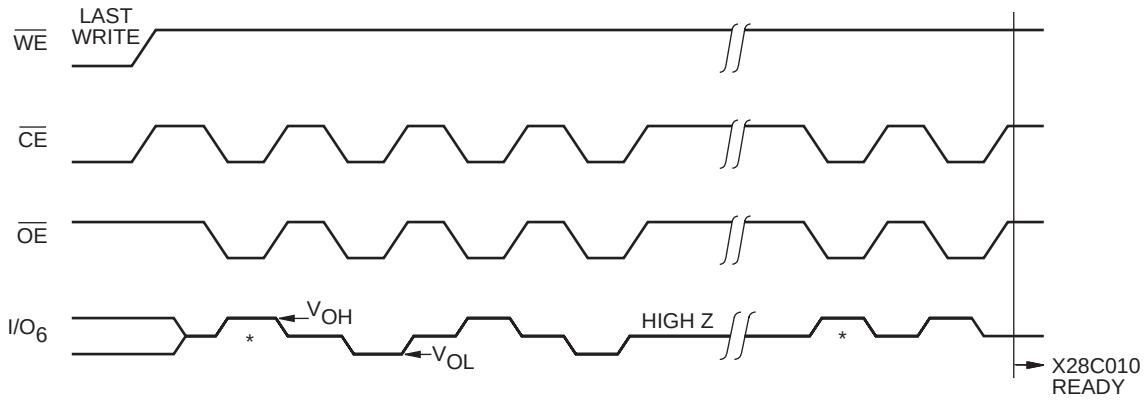
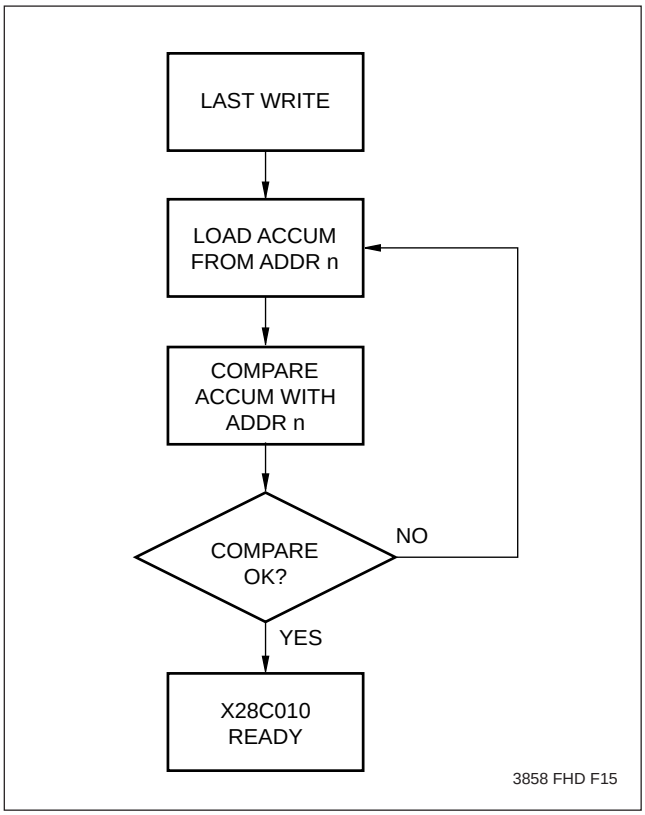



**Figure 5. Toggle Bit Software Flow**




The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

## HARDWARE DATA PROTECTION

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default $V_{CC}$ Sense—All functions are inhibited when $V_{CC}$ is ≤3.5V.
- Write inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

## SOFTWARE DATA PROTECTION

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED: that is the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once $V_{CC}$ was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

## SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

**Software Data Protection**

**Figure 6. Timing Sequence—Byte or Page Write**

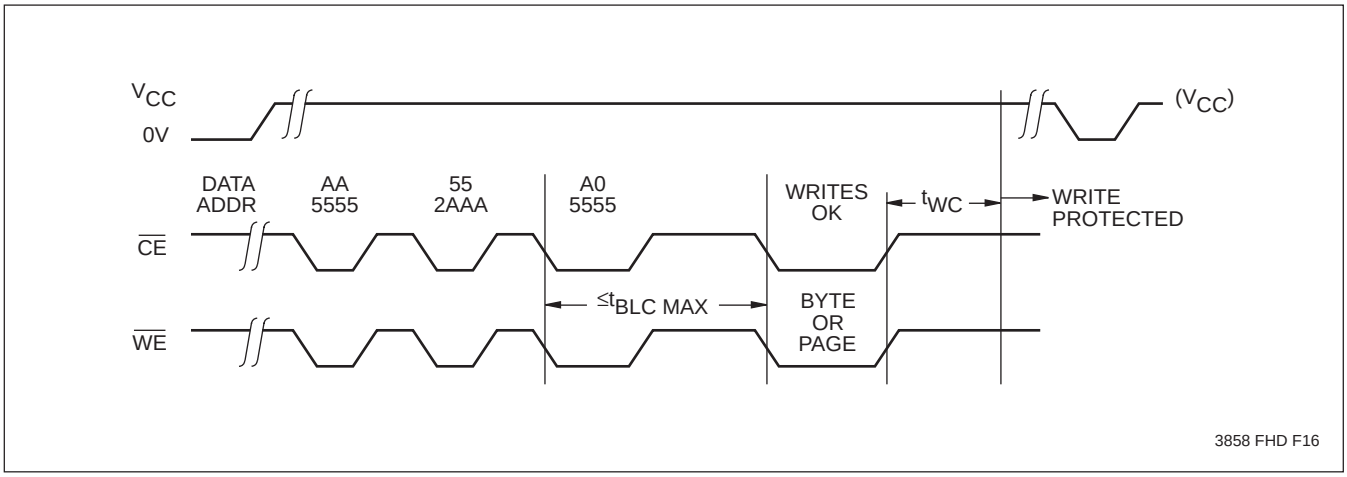
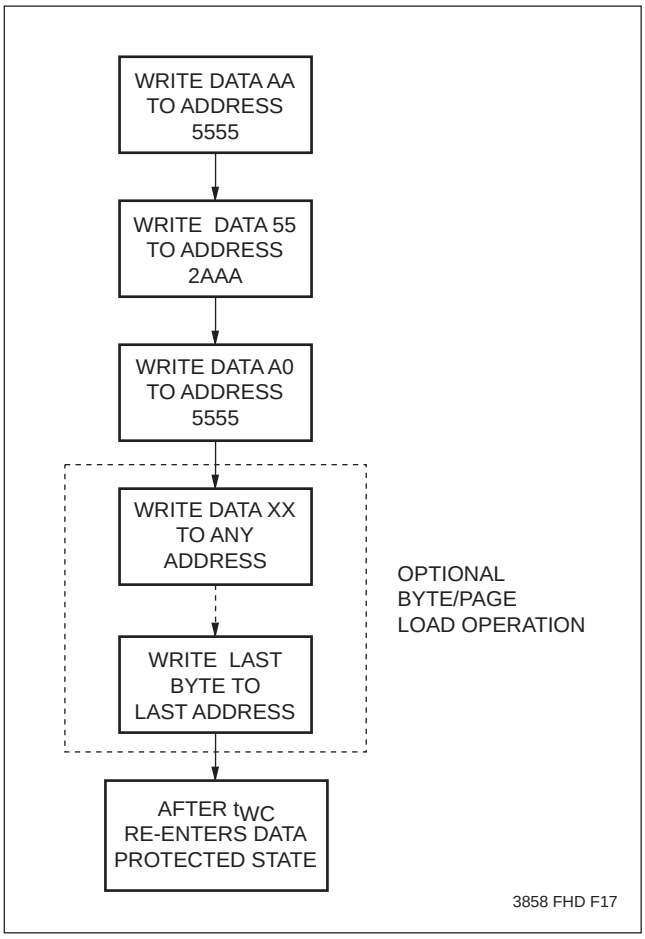



**Figure 7. Write Sequence for Software Data Protection**


WRITE DATA AA TO ADDRESS 5555
WRITE DATA 55 TO ADDRESS 2AAA
WRITE DATA A0 TO ADDRESS 5555
WRITE DATA XX TO ANY ADDRESS
WRITE LAST BYTE TO LAST ADDRESS
OPTIONAL BYTE/PAGE LOAD OPERATION
AFTER $t_{WC}$ RE-ENTERS DATA PROTECTED STATE
3858 FHD F17

Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up. The state of $A_{15}$ and $A_{16}$ while executing the algorithm is don't care.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

### Resetting Software Data Protection

**Figure 8. Reset Software Data Protection Timing Sequence**

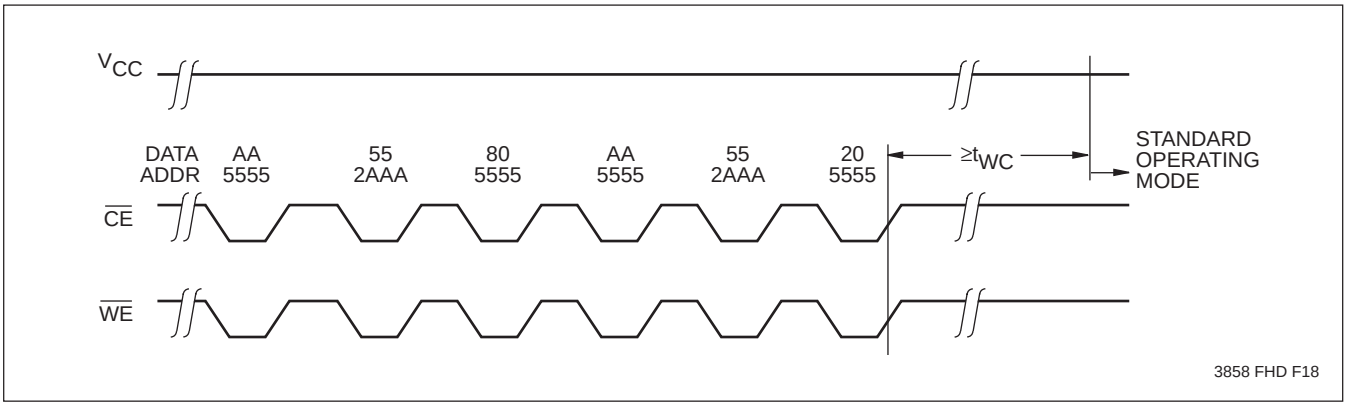
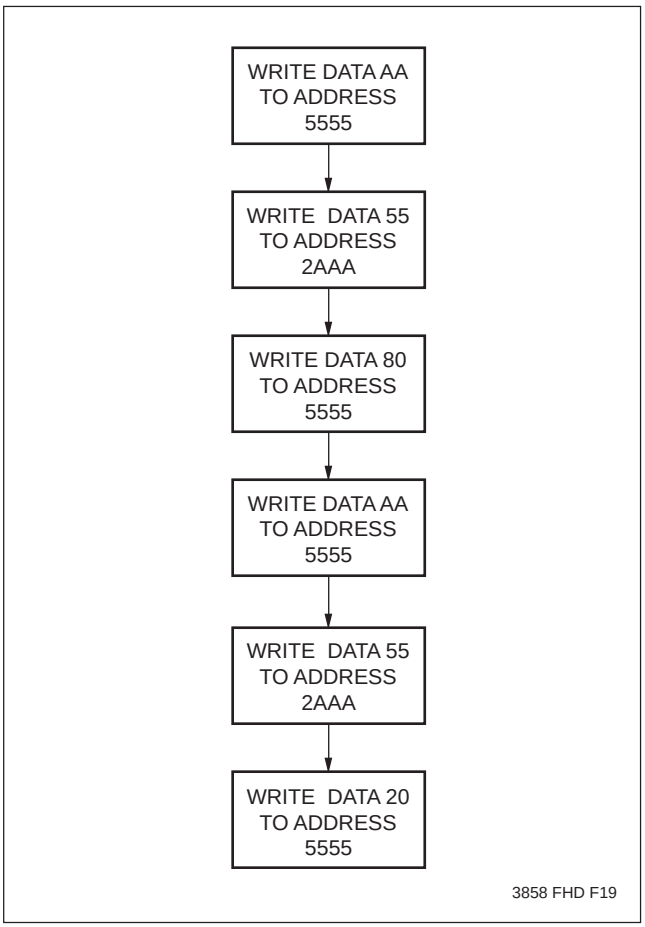



**Figure 9. Software Sequence to Deactivate Software Data Protection**


WRITE DATA AA TO ADDRESS 5555
WRITE DATA 55 TO ADDRESS 2AAA
WRITE DATA 80 TO ADDRESS 5555
WRITE DATA AA TO ADDRESS 5555
WRITE DATA 55 TO ADDRESS 2AAA
WRITE DATA 20 TO ADDRESS 5555
3858 FHD F19

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After $t_{WC}$, the X28C010 will be in standard operating mode.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

## SYSTEM CONSIDERATIONS

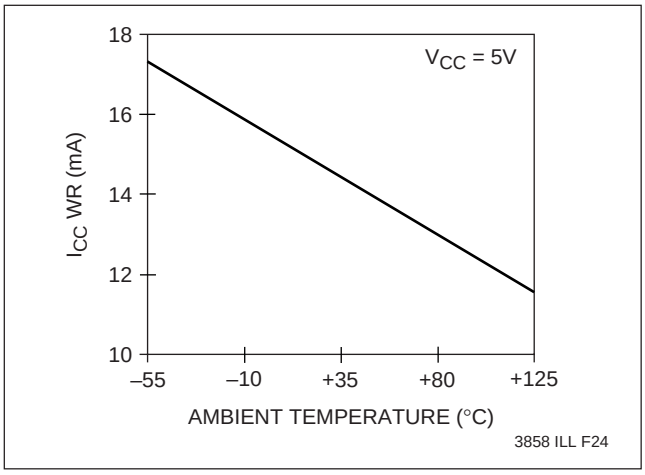
Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

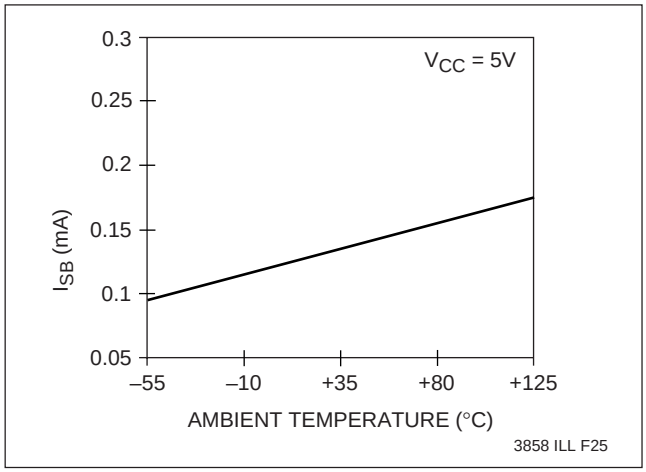
Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between $V_{CC}$ and $V_{SS}$ at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between $V_{CC}$ and $V_{SS}$ for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

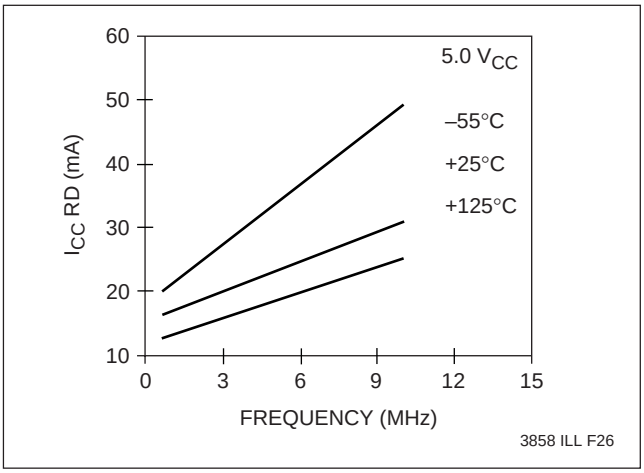
**Active Supply Current vs. Ambient Temperature**




**Standby Supply Current vs. Ambient Temperature**




**$I_{CC}$ (RD) by Temperature over Frequency**



**ABSOLUTE MAXIMUM RATINGS***

Temperature under Bias
- X28C010 ..... –10°C to +85°C
- X28C010I ..... –65°C to +135°C
- X28C010M ..... –65°C to +135°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with
- Respect to $V_{SS}$ ..... –1V to +7V

D.C. Output Current ..... 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMEND OPERATING CONDITIONS**

| Temperature | Min. | Max. |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | –40°C | +85°C |
| Military | –55°C | +125°C |

3858 PGM T02

| Supply Voltage | Limits |
|---|---|
| X28C010 | 5V ±10% |

3858 PGM T03

**D.C. OPERATING CHARACTERISTICS** (Over the recommended operating conditions, unless otherwise specified.)

| Symbol | Parameter | Limits | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $I_{CC}$ | $V_{CC}$ Current (Active) (TTL Inputs) | | 50 | mA | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz |
| $I_{SB1}$ | $V_{CC}$ Current (Standby) (TTL Inputs) | | 3 | mA | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ All I/O's = Open, Other Inputs = $V_{IH}$ |
| $I_{SB2}$ | $V_{CC}$ Current (Standby) (CMOS Inputs) | | 500 | µA | $\overline{CE}$ = $V_{CC}$ – 0.3V, $\overline{OE}$ = $V_{IL}$ All I/O's = Open, Other Inputs = $V_{CC}$ |
| $I_{LI}$ | Input Leakage Current | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$, $\overline{CE}$ = $V_{IH}$ |
| $V_{IL}$(1) | Input LOW Voltage | –1 | 0.8 | V | |
| $V_{IH}$(1) | Input HIGH Voltage | 2 | $V_{CC}$ + 1 | V | |
| $V_{OL}$ | Output LOW Voltage | | 0.4 | V | $I_{OL}$ = 2.1mA |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | V | $I_{OH}$ = –400µA |

3858 PGM T04.2

**Notes:** (1) $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.

## POWER-UP TIMING

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $t_{PUR}$(2) | Power-up to Read Operation | 100 | µs |
| $t_{PUW}$(2) | Power-up to Write Operation | 5 | ms |

3858 PGM T05

## CAPACITANCE $T_A$ = +25°C, f = 1MHz, $V_{CC}$ = 5V

| Symbol | Parameter | Max. | Units | Test Conditions |
|---|---|---|---|---|
| $C_{I/O}$(2) | Input/Output Capacitance | 10 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$(2) | Input Capacitance | 10 | pF | $V_{IN}$ = 0V |

3858 PGM T06

## ENDURANCE AND DATA RETENTION

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Endurance | 10,000 | | Cycles Per Byte |
| Endurance | 100,000 | | Cycles Per Page |
| Data Retention | 100 | | Years |

3858 PGM T07.1

## A.C. CONDITIONS OF TEST

| | |
|---|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 10ns |
| Input and Output Timing Levels | 1.5V |

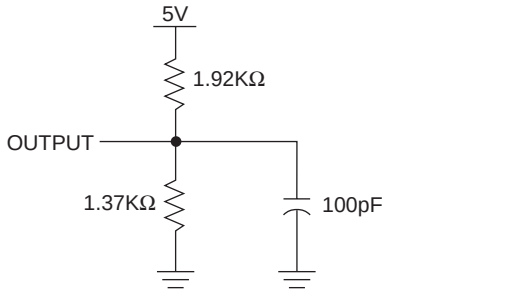
3858 PGM T05.1

## MODE SELECTION

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | I/O | Power |
|---|---|---|---|---|---|
| L | L | H | Read | $D_{OUT}$ | Active |
| L | H | L | Write | $D_{IN}$ | Active |
| H | X | X | Standby and Write Inhibit | High Z | Standby |
| X | L | X | Write Inhibit | — | — |
| X | X | H | Write Inhibit | — | — |

3858 PGM T08

## EQUIVALENT A.C. LOAD CIRCUIT




3858 FHD F04.3

## SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

**Note:** (2) This parameter is periodically sampled and not 100% tested.

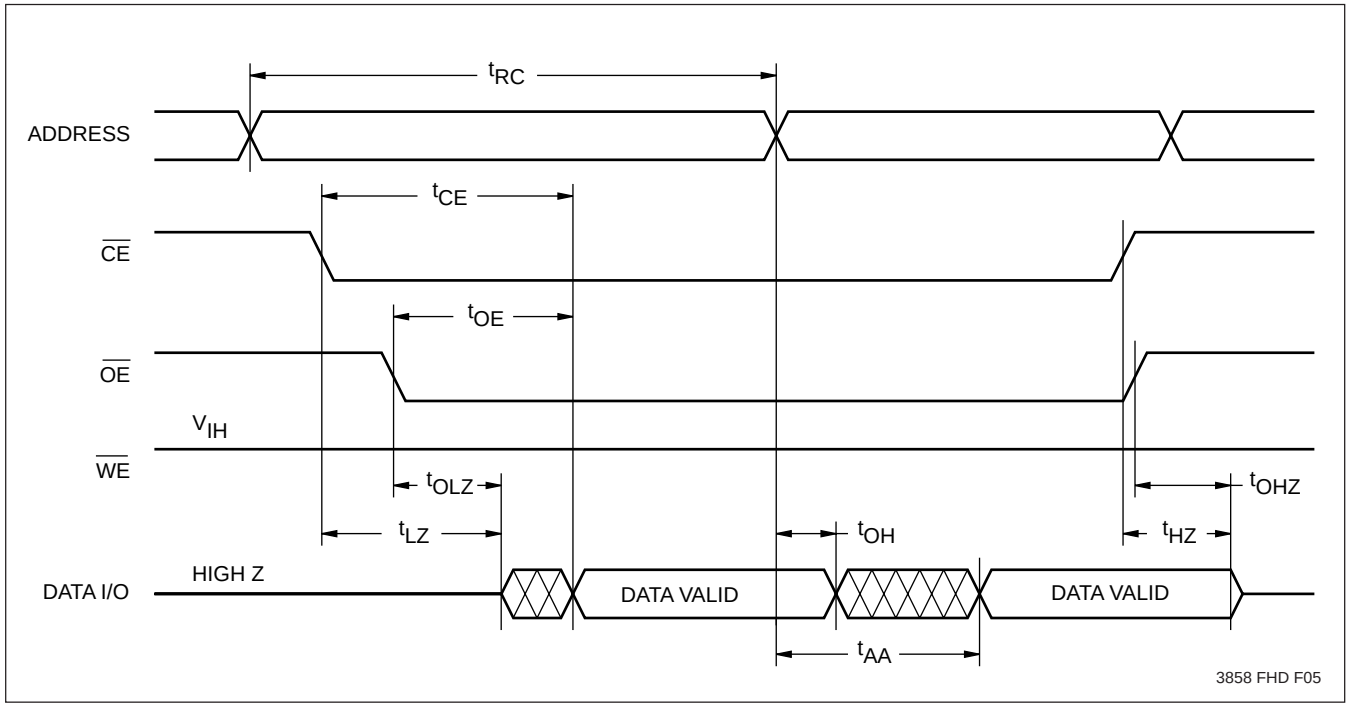
**A.C. CHARACTERISTICS** (Over the recommended operating conditions, unless otherwise specified.)

**Read Cycle Limits**

| Symbol | Parameter | X28C010-12 | | X28C010-15 | | X28C010-20 | | X28C010-25 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 120 | | 150 | | 200 | | 250 | | ns |
| $t_{CE}$ | Chip Enable Access Time | | 120 | | 150 | | 200 | | 250 | ns |
| $t_{AA}$ | Address Access Time | | 120 | | 150 | | 200 | | 250 | ns |
| $t_{OE}$ | Output Enable Access Time | | 50 | | 50 | | 50 | | 50 | ns |
| $t_{LZ}$(3) | $\overline{CE}$ LOW to Active Output | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OLZ}$(3) | $\overline{OE}$ LOW to Active Output | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZ}$(3) | $\overline{CE}$ HIGH to High Z Output | | 50 | | 50 | | 50 | | 50 | ns |
| $t_{OHZ}$(3) | $\overline{OE}$ HIGH to High Z Output | | 50 | | 50 | | 50 | | 50 | ns |
| $t_{OH}$ | Output Hold from Address Change | 0 | | 0 | | 0 | | 0 | | ns |

3858 PGM T09.1

**Read Cycle**



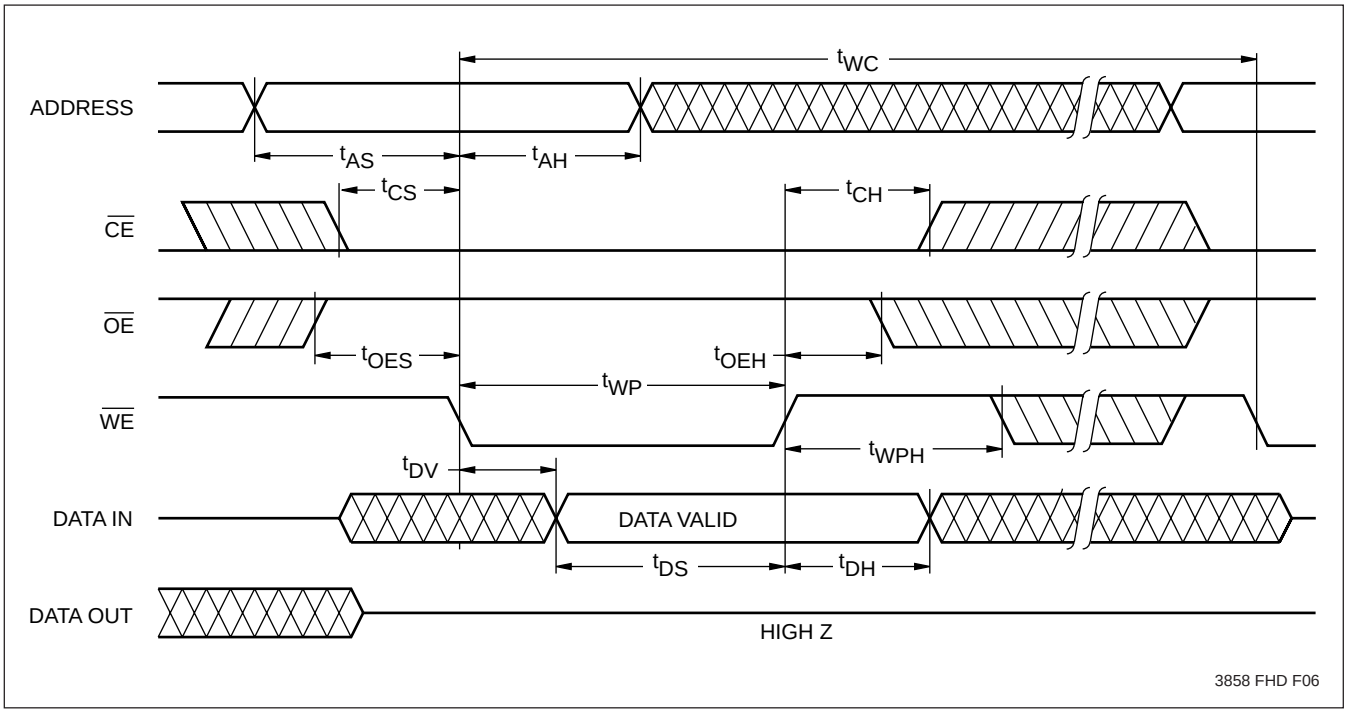

**Note:** (3) $t_{LZ}$ min.,$t_{HZ}$, $t_{OLZ}$ min., and $t_{OHZ}$ are periodically sampled and not 100% tested. $t_{HZ}$ max. and $t_{OHZ}$ max. are measured, with $C_L$ = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

### Write Cycle Limits

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{WC}$(4) | Write Cycle Time | | 10 | ms |
| $t_{AS}$ | Address Setup Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{CS}$ | Write Setup Time | 0 | | ns |
| $t_{CH}$ | Write Hold Time | 0 | | ns |
| $t_{CW}$ | $\overline{CE}$ Pulse Width | 100 | | ns |
| $t_{OES}$ | $\overline{OE}$ HIGH Setup Time | 10 | | ns |
| $t_{OEH}$ | $\overline{OE}$ HIGH Hold Time | 10 | | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 100 | | ns |
| $t_{WPH}$ | $\overline{WE}$ HIGH Recovery | 100 | | ns |
| $t_{DV}$ | Data Valid | | 1 | µs |
| $t_{DS}$ | Data Setup | 50 | | ns |
| $t_{DH}$ | Data Hold | 0 | | ns |
| $t_{DW}$ | Delay to Next Write | 10 | | µs |
| $t_{BLC}$ | Byte Load Cycle | 0.2 | 100 | µs |

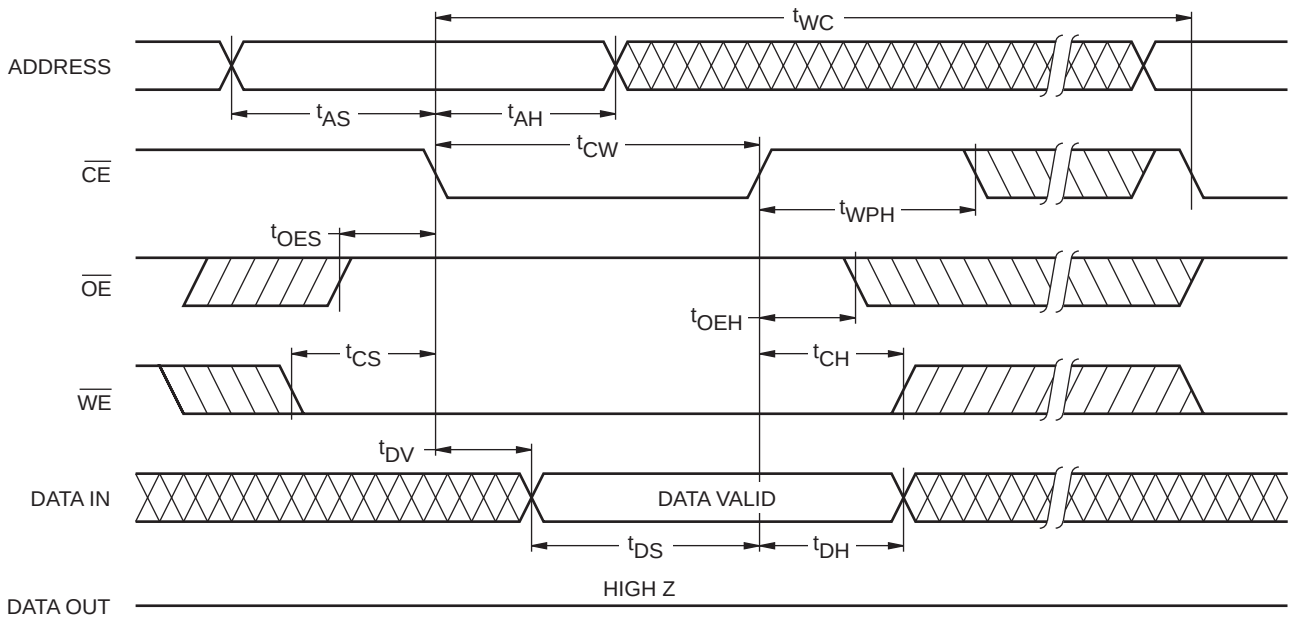
3858 PGM T10.1

### $\overline{WE}$ Controlled Write Cycle

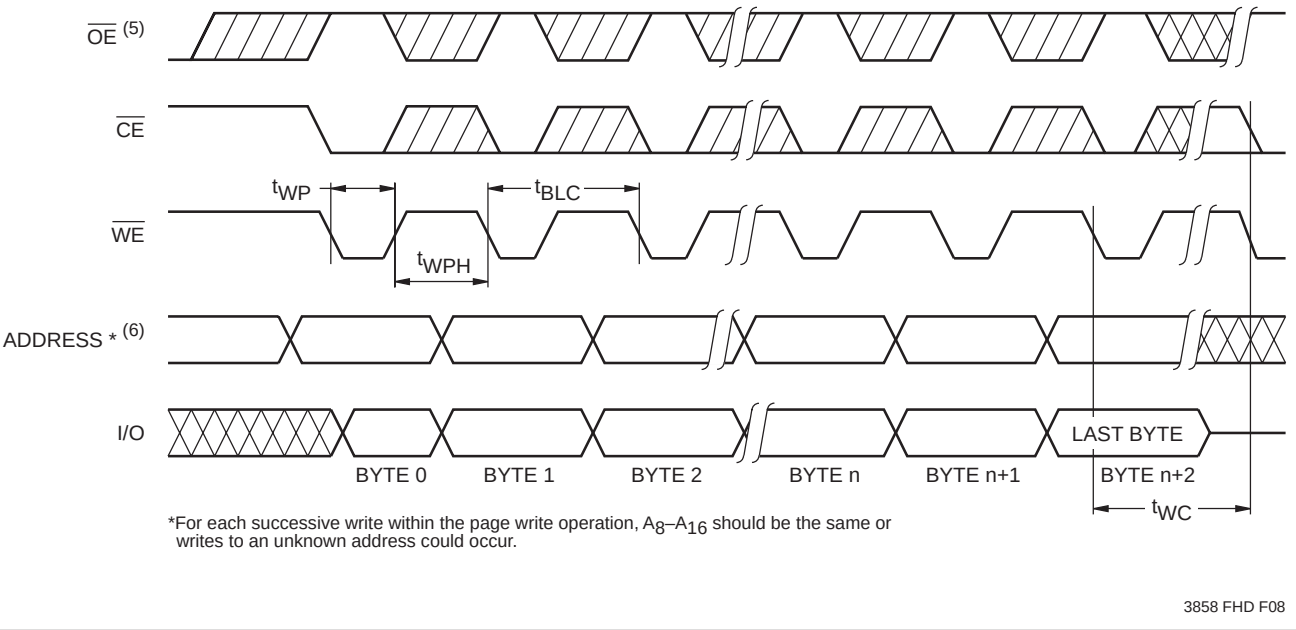



**Notes:** (4) $t_{WC}$ is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

## $\overline{CE}$ Controlled Write Cycle



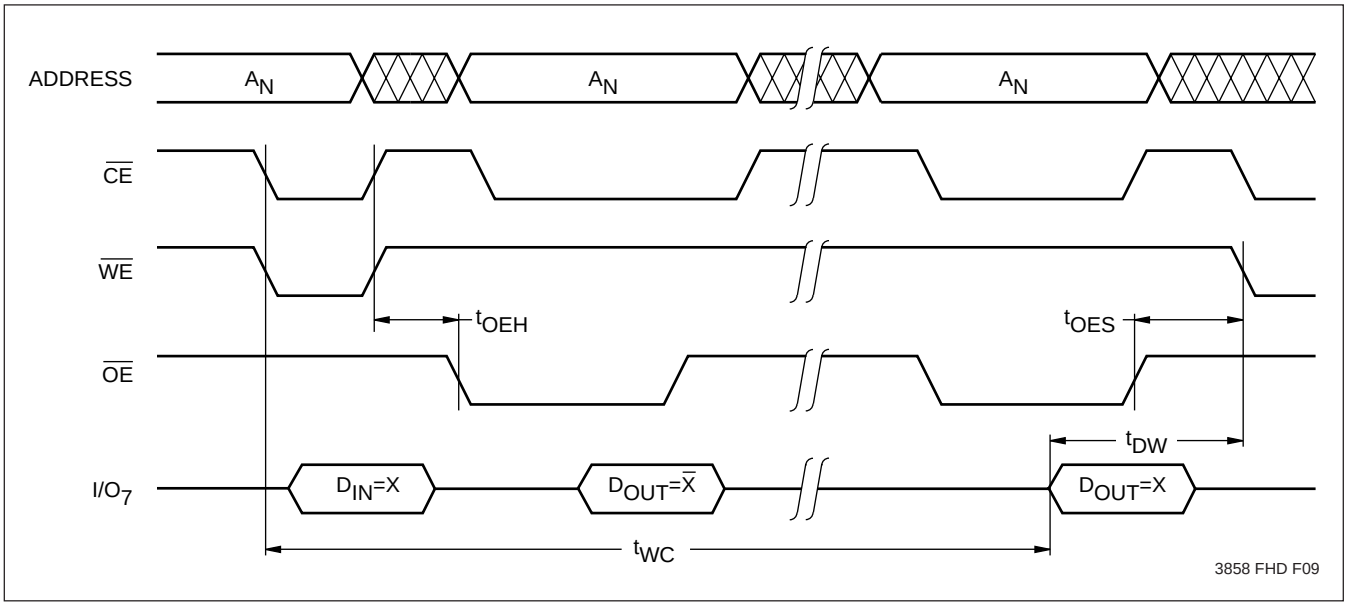

## Page Write Cycle



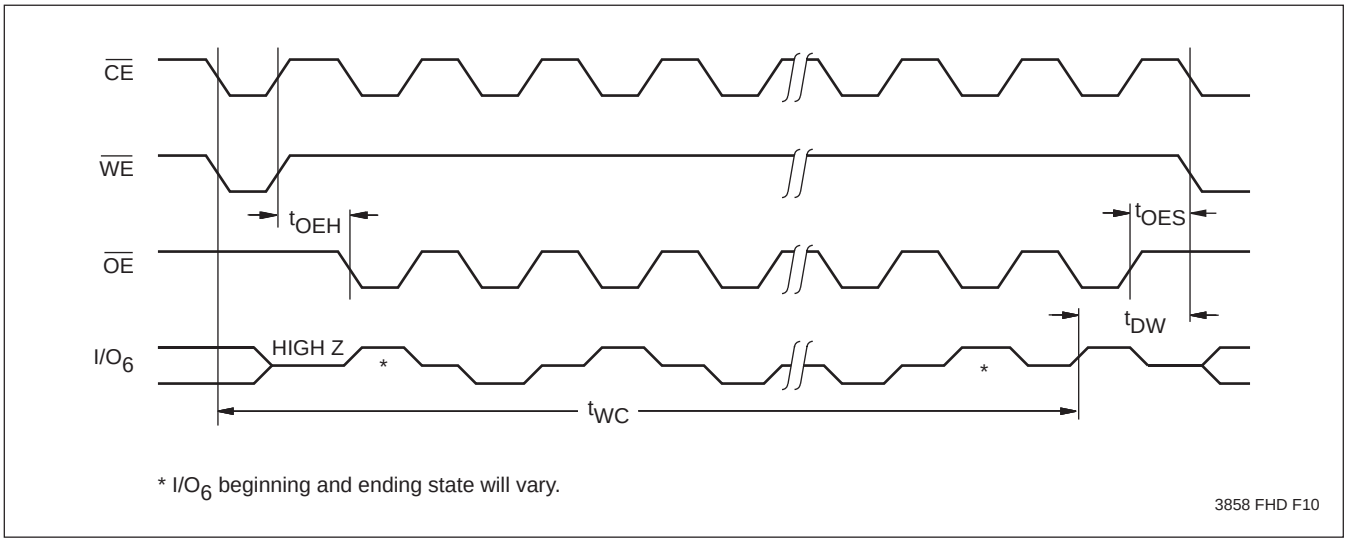

**Notes:** (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

### $\overline{\text{DATA}}$ Polling Timing Diagram(7)




### Toggle Bit Timing Diagram

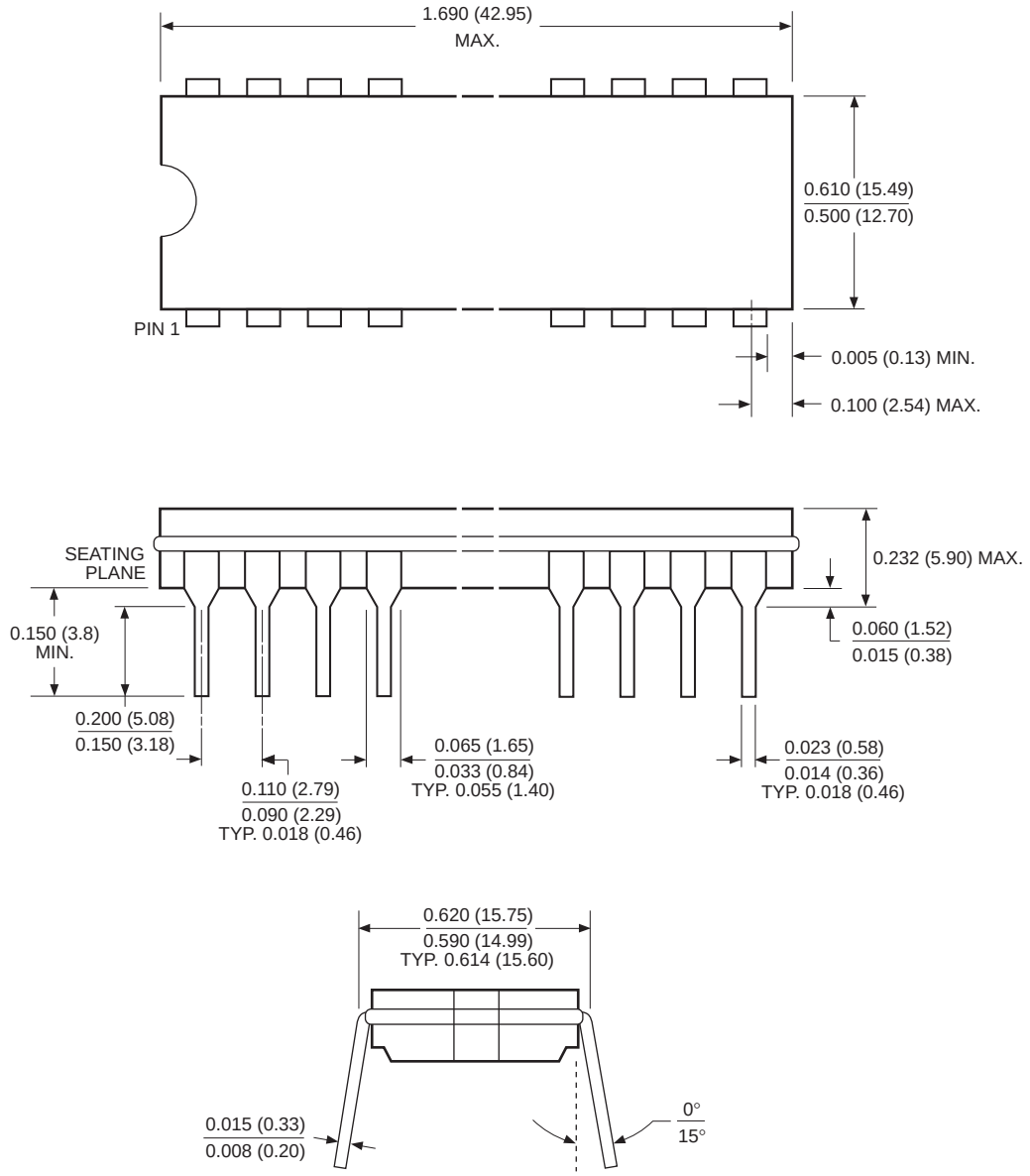



**Note:** (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

**NOTES**

## PACKAGING INFORMATION

### 32-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

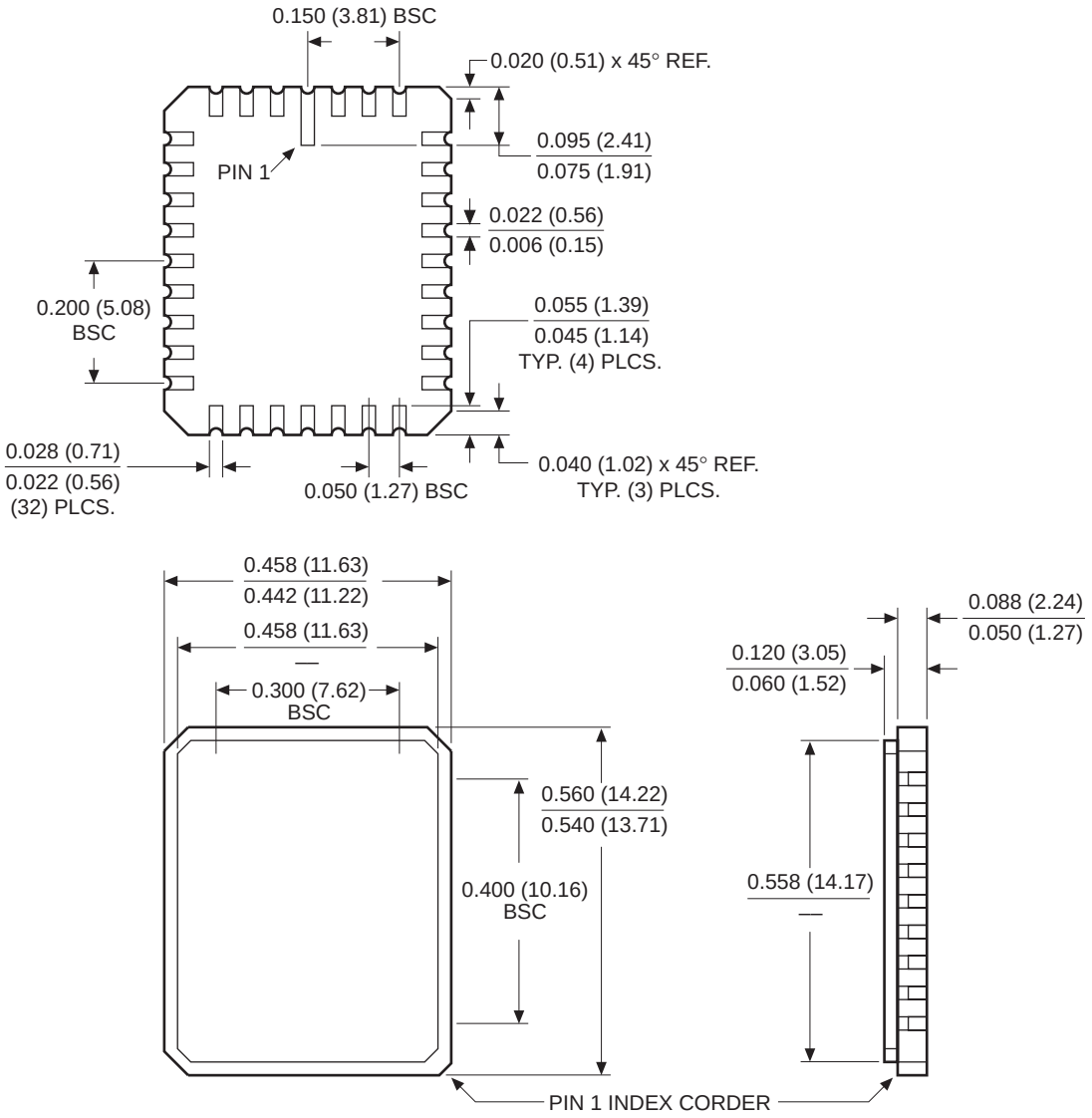



**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

3926 FHD F09

## PACKAGING INFORMATION

### 32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



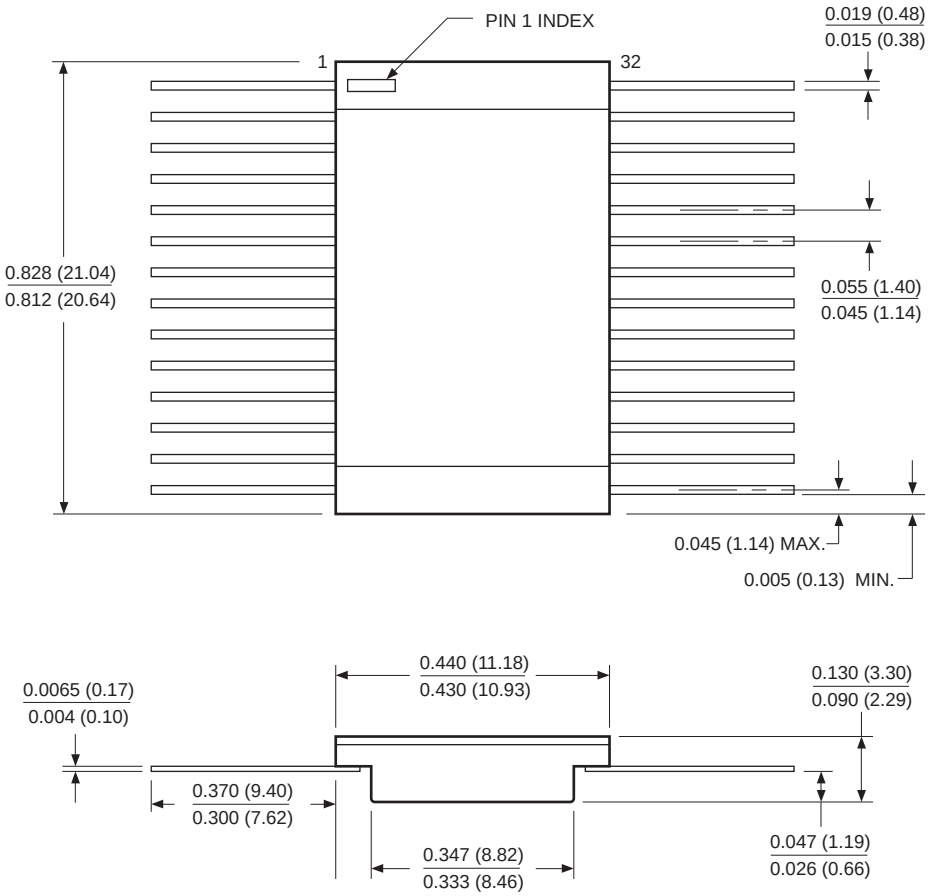

**NOTE:**

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

3926 FHD F14

## PACKAGING INFORMATION

### 32-LEAD CERAMIC FLAT PACK

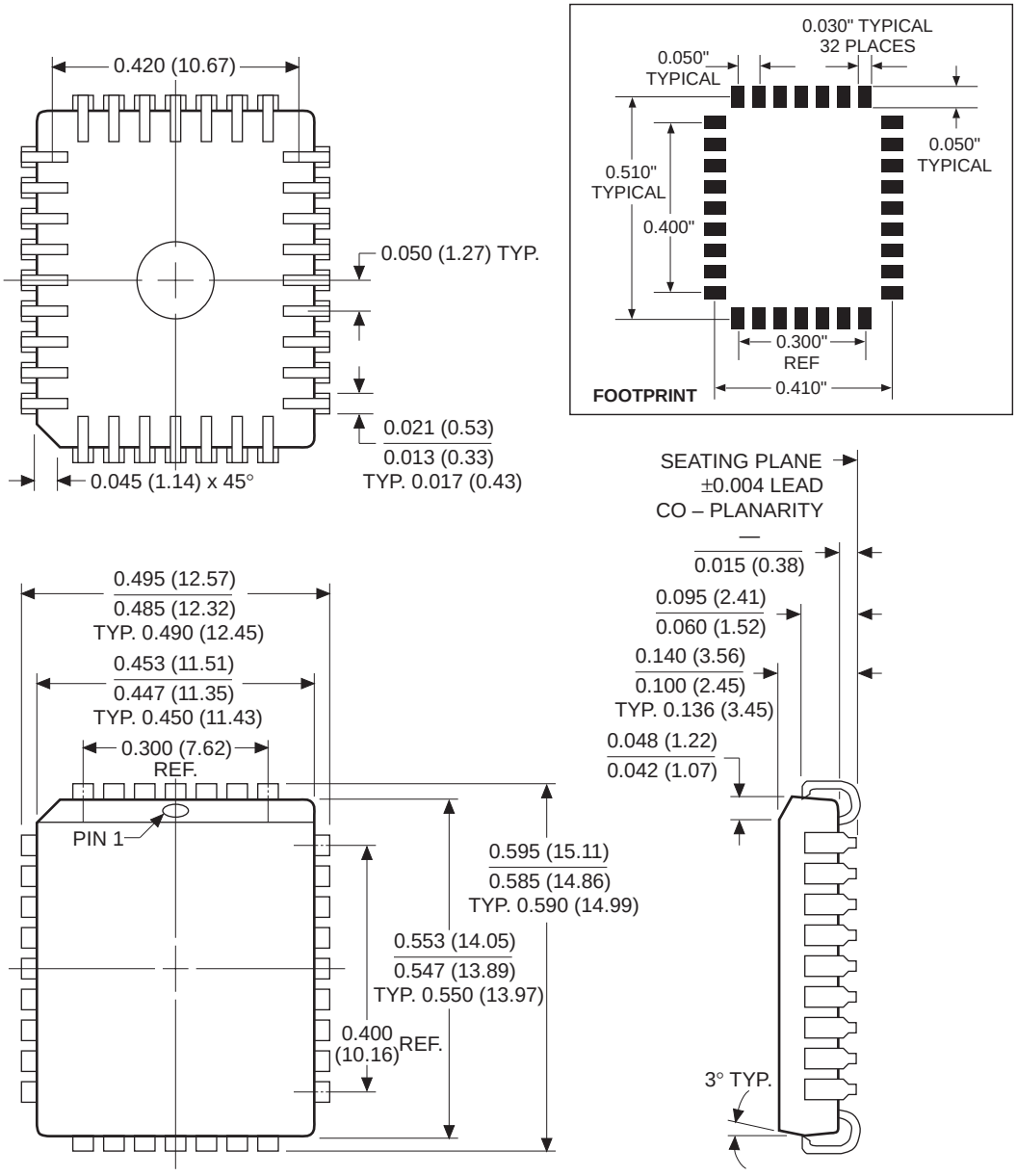



**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

3926 FHD F20

## PACKAGING INFORMATION

### 32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J




**NOTES:**

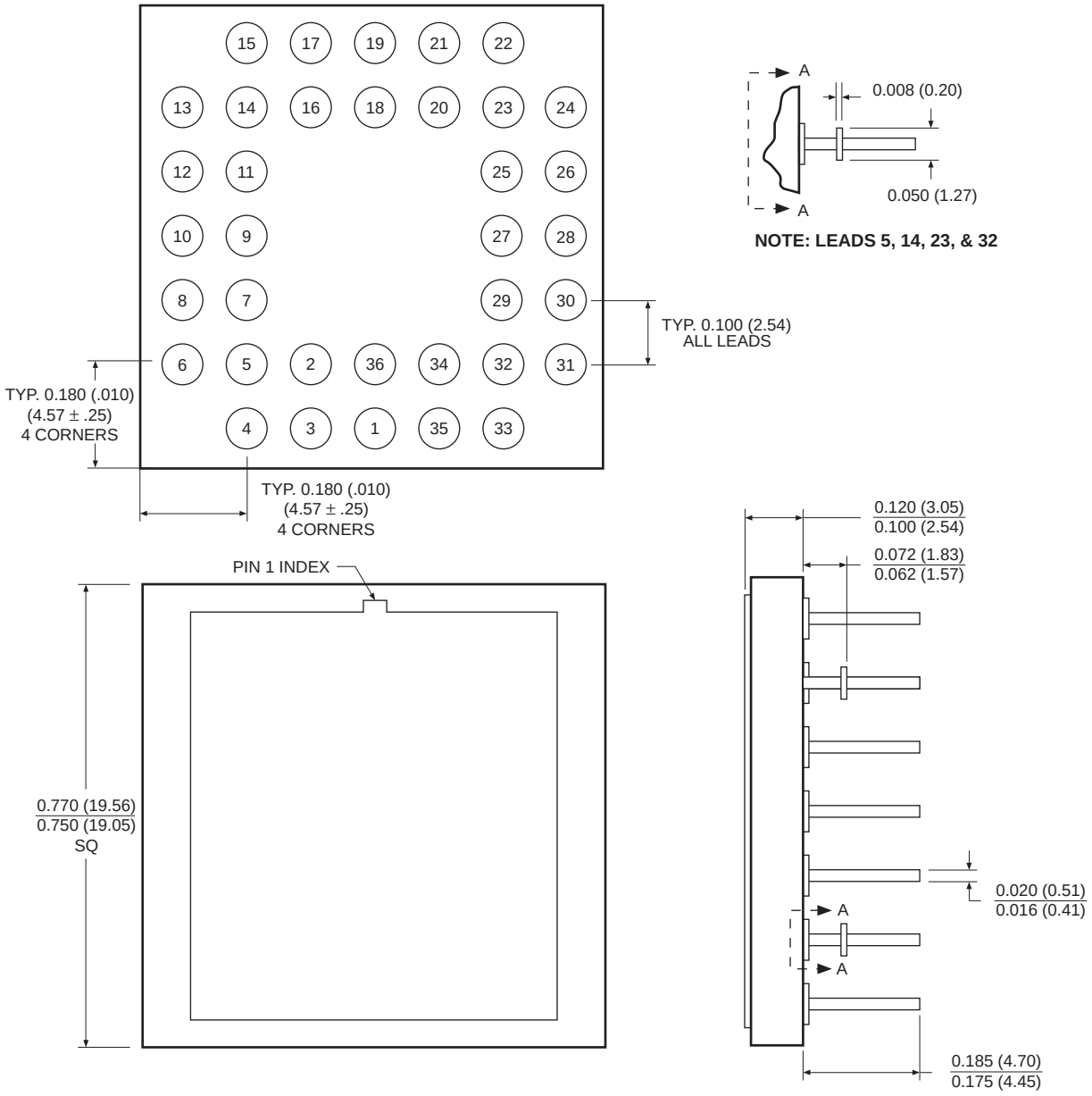
**1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

**2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

3926 FHD F13

## PACKAGING INFORMATION

### 36-LEAD CERAMIC PIN GRID ARRAY PACKAGE TYPE K

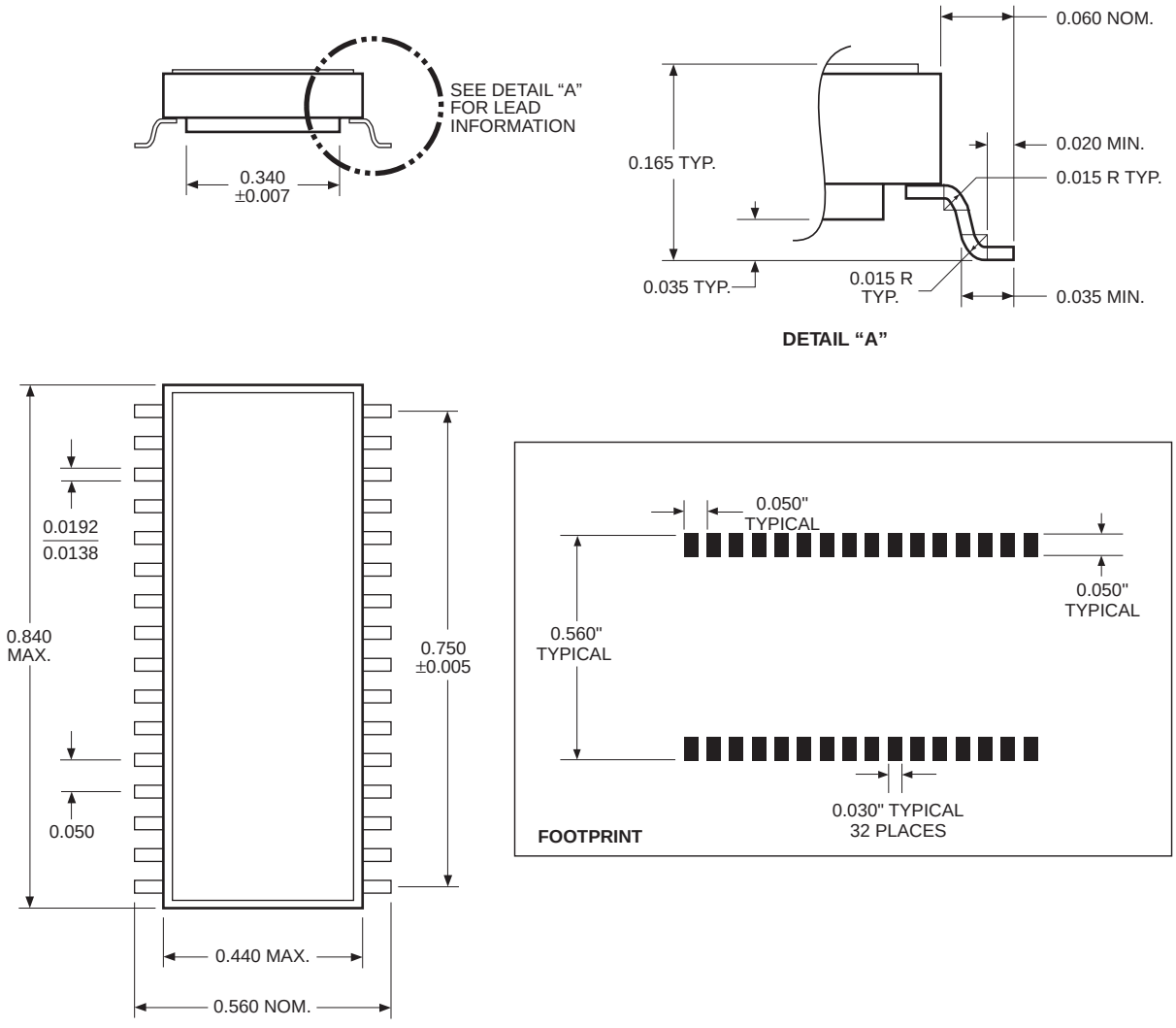



**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

3926 FHD F21

## PACKAGING INFORMATION

### 32-LEAD CERAMIC SMALL OUTLINE GULL WING PACKAGE TYPE R

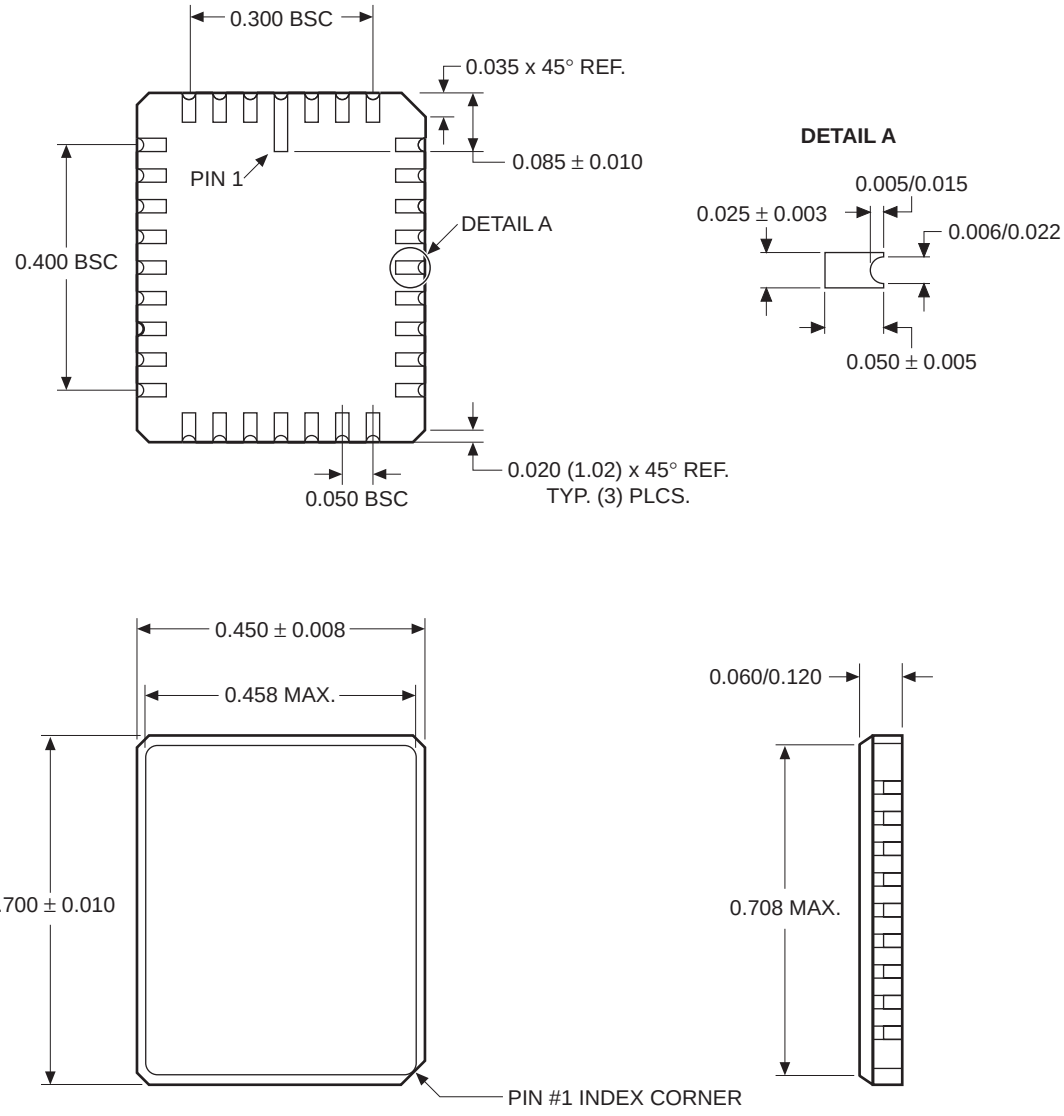



**NOTES:**
**1. ALL DIMENSIONS IN INCHES**
**2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES**

3926 FHD F27

## PACKAGING INFORMATION

### 32-PAD STRETCHED CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE N



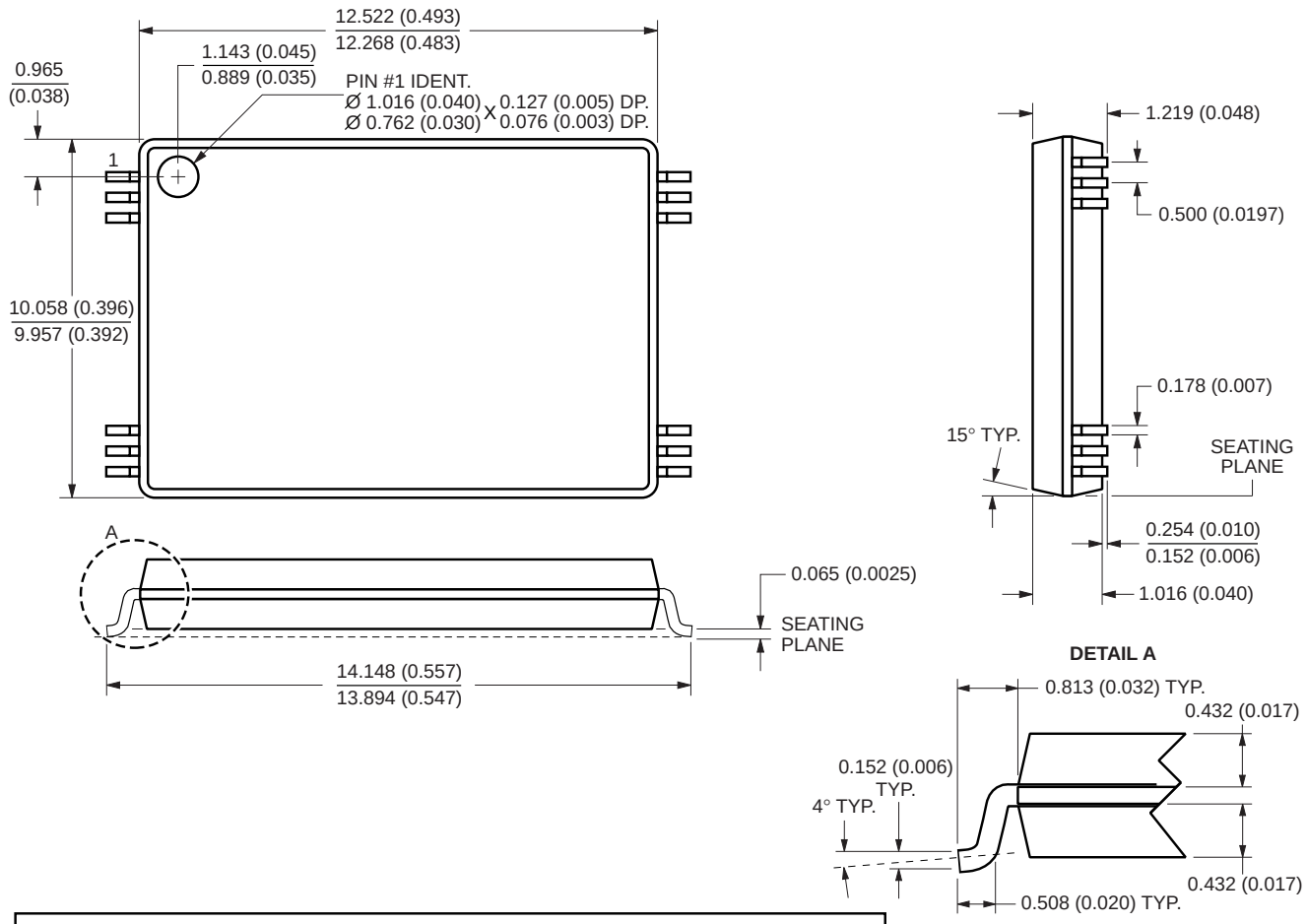

**NOTE:**

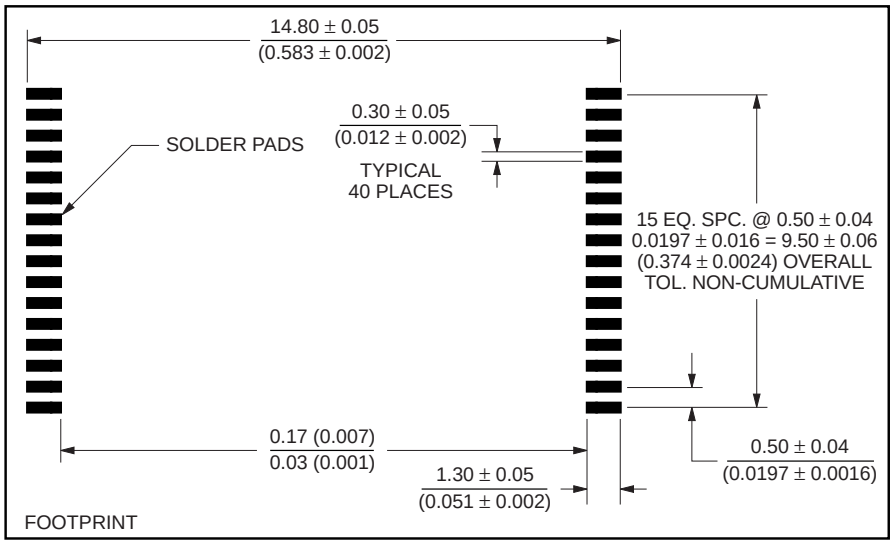
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

3926 FHD F35

## PACKAGING INFORMATION

### 40-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) TYPE T

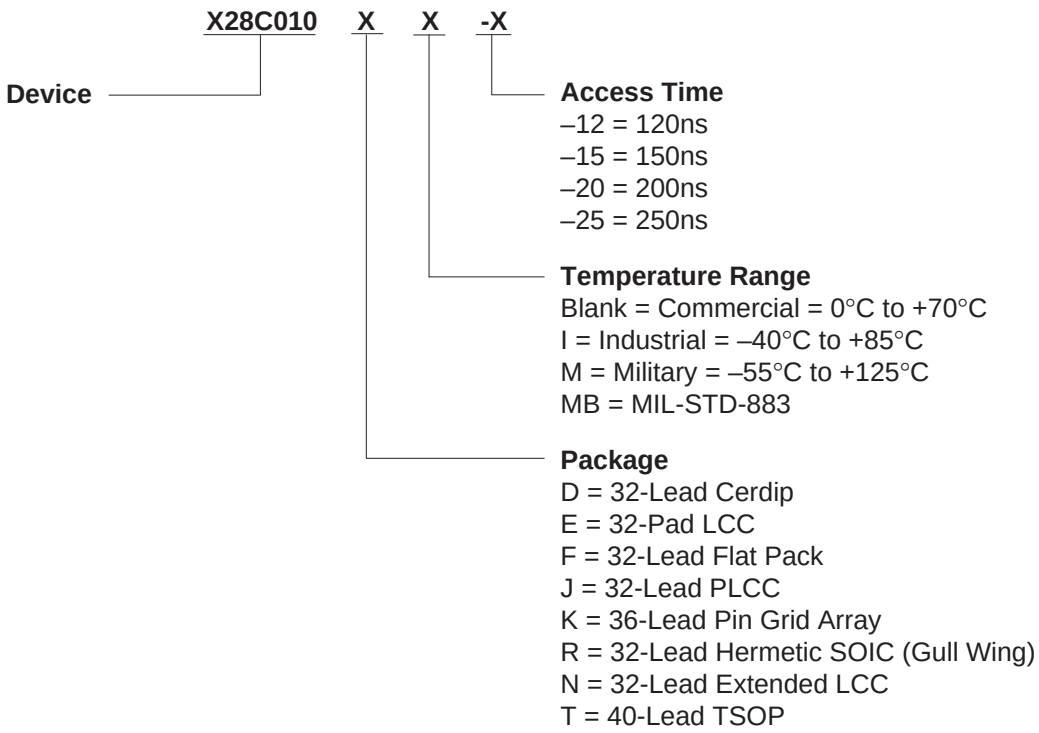



**NOTE:**
**1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).**

3926 ILL F39.2

## ORDERING INFORMATION


X28C010 X X -X
Device
Access Time
–12 = 120ns
–15 = 150ns
–20 = 200ns
–25 = 250ns
Temperature Range
Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
M = Military = –55°C to +125°C
MB = MIL-STD-883
Package
D = 32-Lead Cerdip
E = 32-Pad LCC
F = 32-Lead Flat Pack
J = 32-Lead PLCC
K = 36-Lead Pin Grid Array
R = 32-Lead Hermetic SOIC (Gull Wing)
N = 32-Lead Extended LCC
T = 40-Lead TSOP

**LIMITED WARRANTY**

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

**U.S. PATENTS**

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

**LIFE RELATED POLICY**

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.